Title of the Invention

Method and apparatus for processing video pictures, in particular for large area flicker effect reduction

Background of the Invention

This is a non-provisional application which claims the benefit of application serial number 09/347,191, filed July 20, 1999.

The invention relates to a method and apparatus for processing video pictures, in particular for large area flicker effect reduction.

More specifically the invention is closely related to a kind of video processing for improving the picture quality of pictures which are displayed on matrix displays like plasma display panels (PDP), display devices with digital micro mirror arrays (DMD) and all kind of displays based on the principle of duty cycle modulation (pulse width modulation) of light emission.

Although plasma display panels are known for many years, plasma displays are encountering a growing interest from TV manufacturers. Indeed, this technology now makes it possible to achieve flat colour panels of large size and with limited depths without any viewing angle constraints. The size of the displays may be much larger than the classical CRT picture tubes would have ever been allowed.

Referring to the latest generation of European TV sets, a lot of work has been made to improve its picture quality. Consequently, there is a strong demand, that a TV set built in a new technology like the plasma display technology has to provide a picture so good or better than the old standard TV technology.

A plasma display panel utilises a matrix array of discharge cells which could only be switched ON or OFF. Also unlike a CRT or LCD in which grey levels are expressed by analogue control of the light emission, in a PDP the grey level is controlled by modulating the number of light pulses per frame. This time-modulation will be integrated by the eye over a period corresponding to the eye time response.
For static pictures, this time-modulation, repeats itself, with a base frequency equal to the frame frequency of the displayed video norm. As known from the CRT-technology, a light emission with base frequency of 50 Hz, introduces large area flicker, which can be eliminated by field repetition in 100Hz CRT TV receivers.

Contrary to the CRTs, where the duty cycle of light emission is very short, the duty cycle of light emission in PDPs is ~50% for middle grey. This reduces the amplitude of the 50Hz frequency component in the spectrum, and thus large area flicker artefact, but due to the larger size of PDPs, with a larger viewing angle, even a reduced large area flicker becomes objectionable in terms of picture quality. The present trend of increasing size and brightness of PDPs, will also contribute to aggravate this problem in the future.

Summary of the Invention

It is an object of the present invention to disclose a method and an apparatus which reduces the large area flicker artefact in PDPs in particular for 50Hz video norms, without incurring extra costs similar to those required by 100Hz TV receivers.

This object is achieved by the measures claimed in claims 1, 5 or 11, 12.

According to the claimed solution in claim 1, the reduction of the large area effect is made by utilising an optimised sub-field organisation for the frame period. The sub-fields of a pixel are organised in two consecutive groups, and to a value of a pixel a code word is assigned which distributes the active sub-field periods equally over the two sub-field groups.

This solution has the effect that the 50Hz frequency component substantially reduced compared to a sub-field organisation where only one sub-field group is used. The repetition of 50Hz heavy lighting periods is substituted by a repetition of 100Hz small lighting periods. By using this method virtually no extra costs are added, except for a slight increase in the PDP control complexity.

In order to be able to display also non-standard video signals with variations in the horizontal line synchronisation signal, like the ones generated by video recorders or video games, a vertical blanking period has also to be used where no sub-field is addressed. Here, it is advantageous when this vertical blanking period is replaced by two vertical blanking periods, inserted between every pair of consecutive sub-field groups. This is similar to what happens in 100Hz CRT based TV receivers.

Advantageously, additional embodiments of the inventive method are disclosed in the respective dependent claims 2 to 4.

Advantageous embodiments for the apparatus disclosed in claim 5 are apparent from the dependent claims 6 to 10.

An inventive method for coding pixel values to achieve corresponding sub-field code words is apparent from claim 11. The corresponding apparatus using these sub-field code words for display driving is claimed in claim 12.

Brief Description of the Drawing

Exemplary embodiments of the invention are illustrated in the drawings and are explained in more detail in the following description.

In the figures:

Fig. 1 shows an illustration for explaining the sub-field concept of a PDP;

Fig. 2 shows a typical sub-field organisation used for 60Hz video standards;

Fig. 3 shows a new sub-field organisation for 50Hz video standards; and

Fig. 4 shows a block diagram of the apparatus according to the invention.

Description of the Preffered Embodiments

In the field of video processing is an 8-bit representation of a luminance level very common. In this case each level will be represented by a combination of the following 8 bits:

$2^0 = 1$, $2^1 = 2$, $2^2 = 4$, $2^3 = 8$, $2^4 = 16$, $2^5 = 32$, $2^6 = 64$, $2^7 = 128$

To realise such a coding scheme with the PDP technology, the frame period will be divided in 8 lighting periods which are also very often referred to sub-fields, each one corresponding to one of the 8 bits. The duration of the light pulse for the bit $2^1 = 2$ is the double of that for the bit $2^0 = 1$. With a combination of these 8 sub-periods, we are able to build said 256 different grey levels. E.g. the grey level 92 will thus have the corresponding digital code word %1011100. It should be

appreciated, that the sub-fields may consist of a number of small pulses with equal amplitude and equal duration. Without motion, the eye of the observer will integrate over about a frame period all the sub-periods and will have the impression of the right grey level. The above-mentioned sub-field organisation is shown in Fig. 1.

Most of the developments for PDPs have been made for 60Hz video standards, like NTSC. For these video standards it has been found that a refined sub-field organisation should better be used to avoid artefacts and improve picture quality.

An example of a commonly used sub-field organisation for 60Hz video standards is shown in Fig. 2. The sub-field number has been increased to 12 sub-fields SF. The relative duration of the sub-fields are given in Fig. 2. When all sub-fields are activated, the lighting phase has a relative duration of 255 relative time units. The value of 255 has been selected in order to be able to continue using the above mentioned 8 bit representation of the luminance level or RGB data which is being used for PDPs. The seven most significant sub-fields have a relative duration of 32 relative time units. In the field of PDP technology, the relative duration of a sub-field is often referred to the 'weight' of a sub-field, the expression will also be used hereinafter. Between each sub-field SF, there is a small time period in which no light is emitted. This time period is used for the addressing of the corresponding plasma cells. After the last sub-field a longer time period where no light is emitted is added. This time period corresponds to the vertical blanking period of the video standard. The implementation of such a vertical blanking period is necessary in order to be able to handle non-standard video signals generated in VCR's or video games, etc.

A digital representation of the grey level 92 in this sub-field organisation is e.g. 000001111100. This figure is a 12 bit binary number corresponding to the 12 sub-fields. It will be used to control the lighting pulses for the corresponding pixel during a frame period. It should be noted, that there exist a few other possible 12 bit code words for the same grey level, due to the fact that there are seven sub-fields width identical weight.

In Fig. 3 a new sub-field organisation according to the invention is shown for 50Hz video standards. The frame period for 60Hz video standards is 16.6ms and for 50Hz 20ms and thus larger for 50Hz video standards. This allows for the addressing of more sub-fields in 50Hz video standards. In the example shown in Fig. 3 the number of sub-fields has been increased to 14. This does not cause extra costs since the added time to the frame period is greater than the added number of sub-fields: (20.0/16.6) > (14/12).

The sub-fields are structured in two separate sub-field groups G1, G2.
One vertical frame blanking period has been replaced by two vertical frame blanking periods VFB1, VFB2, one at the end of the frame period and the other between the two sub-field groups.
The 2 sub-field groups are identical in terms of the six most significant sub-fields and different in terms of the least significant sub-field. The weight of the least significant sub-field is small and does not introduce significant large area flicker, and this is the reason why it is not necessary that they are also identical.

For large area flicker effect reduction a sub-field coding process that distributes luminance weight of a given pixel value symmetrically over the 2 sub-field groups is also ap-

plied. A small difference in luminance weight between the 2 sub-field groups, means a small 50 Hz luminance frequency component, and thus small levels of large area flicker. For the sub-field coding process there is no need of a complicated calculation. A corresponding table where the code words for the 256 different grey levels/pixel values are stored can be used.

The coding process can best be explained with an example. Consider the grey level/pixel value 87. This number can be written in the following form:

87 = 3 + 44 +40

87 has been split in three components. The first component, 3 = (87 mod 4) is the component which is to be coded by the least significant sub-fields of the two sub-field groups. The second and third component, which must be multiples of 4 (because of the fact that the six most significant sub-fields in both groups have weights which are multiples of four) are made as equal as possible. If they cannot be made equal, as this is the case with **87**, the second component, to be coded with the sub-fields of group 1, should be made greater by 4. In the example, **44** is to be coded with the sub-fields of group G1, and **40** is to be coded with the sub-fields of group 2. Using these rules, the final code is:

87 =

1 * 1 + 1 * 4 + 0 * 8 + 1 * 16 + 1 * 24 + 0 * 32 + 0 * 40

1 * 2 + 0 * 4 + 0 * 8 + 1 * 16 + 1 * 24 + 0 * 32 + 0 * 40

or

87 = 45 + 42

45 = 1 + 4 + 16 + 24 (Group 1)

42 = 2 + 16 + 24 (Group 2)

or

87 = 00110010011011.

With this coding process, the difference in weight between the two sub-field groups is never greater than 5.

A second example will be explained with grey level/pixel value **92**.

92 = 0 + 48 +44

⇒

92 =

0 * 1 + 0 * 4 + 1 * 8 + 1 * 16 + 1 * 24 + 0 * 32 + 0 * 40

0 * 2 + 1 * 4 + 0 * 8 + 1 * 16 + 1 * 24 + 0 * 32 + 0 * 40

or

92 = 48 + 44

48 = 8 + 16 + 24 (Group 1)

44 = 4 + 16 + 24 (Group 2)

or

92 = 00110100011100.

An apparatus according to the invention is shown in Fig. 4. The apparatus may be integrated together with the PDP matrix display. It could also be in a separate box which is to be connected with the plasma display panel. Reference no. 10 denotes the whole apparatus. The video signal is fed to the apparatus via the input line V_{in}. Reference no. 11 denotes a video processing unit, wherein the video signal is digitalized and Y,U, V data is produced. As plasma displays are addressed in progressive scan mode, interlace video standards require a previous conversion, here. For interlace - progressive scan conversion many solutions are known in the art which can be used here. Also, an YUV/RGB data conversion will be made in this unit as the PDPs work with RGB data. The generated RGB data is forwarded to the sub-field coding unit 12. Therein, to each RGB pixel value the corresponding code word will be selected from a table 13. These code words are forwarded to the frame memory in addressing unit 14 of the PDP 10. With these data the addressing unit 14 controls the plasma display 15.

For 60Hz video norms the large area flicker effect is not so disturbing as for 50Hz video standards. While the invention has been explained for 50Hz video norms it is apparent, that it can also be used to improve the picture quality of 60Hz video norms.

The blocks shown in Fig. 4 can be implemented with appropriate computer programs rather than with hardware components.

The invention is not restricted to the disclosed embodiments. Various modifications are possible and are considered to fall within the scope of the claims. E.g. the number and weights of the used sub-fields can vary from implementation to implementation.

All kinds of displays which are controlled by using different a PWM like control for grey-level variation can be used in connection with this invention.